

**REMARKS**

The Examiner's withdrawal of the objections to the claims, the title, and the drawings in the "DETAILED ACTION" is noted with appreciation. It is acknowledged that any enablement and indefiniteness rejections were also indicated in the current Office Action to have been overcome by the previous Reply.

However, it is noted that on the "Office Action Summary" form at item "10)", it appears that the box indicating that the Examiner objects to the drawings has inadvertently remained marked. If this is an oversight, it is respectfully requested that the objection box be unmarked and that the approval box be marked in the next communication from the Office. Otherwise, it is respectfully requested that a clarification be provided.

Claims 1-73 are presently pending in the instant Application. Although no claims are canceled, amended, or added by this Reply, the pending claims are reproduced above in final form for the convenience of the Office.

With the current and final Office Action, claims 33-42, 47, and 54 were allowed. Claims 1-32, 43-46, 48-53, and 55-73 were rejected "under 35 U.S.C. 103(a) as being unpatentable over Manning (USPN 6,288,954) in view of Kajigaya et al. (USPN 5,426,616)."

1           Of the pending claims 1-73, claims 1, 17, 33, 43, 47, 53, 54, 60, and 63 are  
2 independent.

3           Of these independent claims, claims 33, 47, and 54 are allowed.

4           The allowability of the six other independent claims 1, 17, 43, 53, 60, and 63  
5 is addressed further below.

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8           Although each pending dependent claim includes additional element(s)  
9 militating toward allowability, it is respectfully submitted that the dependent claims  
10 are allowable at least for the reasons given below in connection with their respective  
11 independent claim 1, 17, 43, 53, 60, or 63.

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14           It is respectfully requested that the following arguments be entered and  
15 considered by the Examiner.

1 I. The rejection of claims 1, 17, 43, 53, 60, and 63 under 35 U.S.C.  
2 103(a) cannot be sustained under the facts or the law.

3  
4 A. There is insufficient motivation to combine Manning and  
5 Kajigaya et al.  
6

7 The current Office Action reads at the last two full sentences on page 2,  
8 “However, Manning does not expressly disclose the details for the circuit to generate  
9 a reference voltage  $V_{ref}$ . Kajigaya et al. disclose, in Figs. 27 and 37, a specific  
10 circuit to generate a reference voltage providing variable gain with high accuracy.”  
11 In contradistinction to the former of the two above-quoted sentences, Fig. 3 of  
12 Manning “is a schematic diagram of an embodiment of the reference-signal  
13 generator of FIG. 2.” (Manning, column 2, lines 57-58.) At column 3, lines 3-5,  
14 Manning reads, “... on-board reference-signal generator 32, which in one  
15 embodiment is used to internally generate a reference signal  $V_{refint}$  during testing of  
16 the circuit.”

17 The disclosure and/or teachings of Manning, particularly with regard to Fig. 3  
18 and the text related thereto, appear to vitiate the obviousness motivation as provided  
19 by the Office Action at the first full sentence on page 3, which reads “Therefore, it  
20 would have been obvious for one skilled in the art to use the specific circuit to  
21 generate a reference voltage of Kajigaya et al. for the broad circuit to generate a  
22 reference voltage of Manning for the expected results of variable gain with high  
23 accuracy.”

24 In summary, Manning includes disclosure (e.g., textual description and  
25 drawings) of details for a reference voltage generator. The reference voltage

1 generator of Manning is simpler and cheaper to implement, and the voltage  
2 generating details of Kajigaya et al. require a greater chip surface area and are more  
3 complex and consequently more costly. Thus, it is respectfully submitted that there  
4 was insufficient motivation at the time of the invention to look to Kajigaya et al. for  
5 details of a reference voltage generator when Manning provided such details; thus,  
6 there was insufficient motivation to combine Manning and Kajigaya et al.

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8 B. Even assuming, *arguendo*, that Manning and Kajigaya et al.  
9 could have been combined for some purpose, any such combination would  
10 not have resulted in the claimed invention.

11  
12 1. Any combination of Manning and Kajigaya et al. would  
13 have resulted in the reference-signal generator 32 of Manning being  
14 replaced by the reference voltage generator (VRG) of Kajigaya et al.,  
15 not the standard voltage generator (VLG) as applied in the Office  
16 Action.

17  
18 The current Office Action reads at the last two full sentences on page 2,  
19 “However, Manning does not expressly disclose the details for the circuit to generate  
20 a reference voltage  $V_{ref}$ . Kajigaya et al. disclose, in Figs. 27 and 37, a specific  
21 circuit to generate a reference voltage providing variable gain with high accuracy.”  
22 In contradistinction to the latter of the two above-quoted sentences, Fig. 27 is  
23 directed to a “STANDARD VOLTAGE GENERATOR (VLG)”, and Fig. 37 is  
24 directed to a “FUSE CIRCUIT (FC)”. (See, Kajigaya et al., Figs. 27 and 37, in  
25 conjunction with the overall view provided by Fig. 35.) Furthermore, Kajigaya et al.

1 separately describes what it terms a reference voltage generator (“REFERENCE  
2 VOLTAGE GENERATOR (VRG)”, Figs. 32 and 35 of Kajigaya et al.).

3 The components of Kajigaya et al. that are applied against the claims by the  
4 Office Action are part of the standard voltage generator (VLG) thereof and not part  
5 of the reference voltage generator (VRG) thereof. Hence, the components of  
6 Kajigaya et al. that are asserted to correspond to claim elements are part of the  
7 standard voltage generator (VLG) thereof and not part of the reference voltage  
8 generator (VRG) of Kajigaya et al. Also, it is respectfully submitted that no  
9 components of the reference voltage generator (VRG) (Fig. 32) of Kajigaya et al.  
10 correspond to elements of the invention as claimed.

11 In other words, even assuming, *arguendo*, that one of ordinary skill in the art  
12 would have combined Manning and Kajigaya et al., one of ordinary skill in the art  
13 would have substituted the reference voltage generator (VRG) of Kajigaya et al in  
14 place of the reference-signal generator 32 of Manning. As noted above, the  
15 reference voltage generator (VRG) of Kajigaya et al. does not have components  
16 corresponding to the claimed elements. Thus, it is respectfully submitted that a  
17 combination of Manning and Kajigaya et al. would not have resulted in the claimed  
18 invention.

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20 2. Any combination of Manning and Kajigaya et al. in a  
21 manner as set forth in the Office Action (which appears to supplant the  
22 reference-signal generator 32 of Manning with the standard voltage  
23 generator (VLG) of Kajigaya et al.) necessarily creates a hypothetical  
24 situation that cannot render the claims obvious.  
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1 By way of example, claim 1 reads in full:

2 1. An integrated circuit, comprising:

3 one or more components, including a feedback component, that  
4 receive a distributed voltage, wherein the feedback component of the  
5 one or more components has substantially similar input characteristics  
6 to at least one other component of the one or more components; and

7 a voltage driver that produces a compensated voltage;

8 wherein the compensated voltage is distributed to form the  
9 distributed voltage at the one or more components, and the distributed  
10 voltage is degraded relative to the compensated voltage; and

11 wherein the voltage driver is responsive to feedback from the  
12 feedback component as derived from the distributed voltage to adjust  
13 the compensated voltage so that the distributed voltage is  
14 approximately equal to a nominal voltage.

15 The Office Action reads in its rejection of claim 1 at the last paragraph  
16 starting at the bottom of page 2 and continuing onto page 3, "This to generate a  
17 reference voltage is seen to include 'a feedback receiver Q9-Q10, R10-R18 and Q58-  
18 Q65, Q49, R1-R9 and Q41-Q48 or Q3)', 'a reference voltage driver (OA1, OA2 or  
19 Q1-Q2 and Q50-Q52)', 'a register (DEC1 and DEC2)' and a counter (CTRN and  
20 CTRB)'."

21 Assuming, *arguendo*, that the above correspondences as set forth in the  
22 Office Action comport with 35 U.S.C. §§ 102 and 103, the 'feedback  
23 component/receiver' of Q9-Q10, R10-R18, and Q58-Q65 receives an output from  
24 the 'reference voltage driver' of OA1. This output of the 'reference voltage driver' is  
25 the voltage between Q7 and Q55 (of op amp OA1 as shown in the standard voltage  
generator (VLG) of Fig. 27 of Kajigaya et al.) and is provided to the 'feedback  
component/receiver' at Q9.

1 For this combination and these correspondences to render claim 1 obvious,  
2 this output voltage must correspond to the **compensated voltage** produced by the  
3 **voltage driver** as recited in claim 1 in the following element(s): **voltage driver that**  
4 **produces a compensated voltage.** Claim 1 further recites **wherein the**  
5 **compensated voltage is distributed to form the distributed voltage at the one or**  
6 **more components, and the distributed voltage is degraded relative to the**  
7 **compensated voltage.**

8 In other words, the output of OA1 would also need to be received at the **one**  
9 **or more components.** This is further reflected by **one or more components,**  
10 **including a feedback component, that receive a distributed voltage** as also  
11 recited in claim 1. Hence, for this aspect of the combination rejection to be  
12 technically consistent, the output of OA1 must also be received at the other (non-  
13 feedback) components.

14 However, the output of OA1 is not provided external of the standard voltage  
15 generator (VLG) in Fig. 27 of Kajigaya et al. Moreover, the rejection in the Office  
16 Action sets forth a correspondence between the “one or data receivers (or  
17 ‘components’) (18 and 24 of Fig. 1 of Manning)” as quoted from the first sentence of  
18 the last paragraph on page 2 of the Office Action. These differential input buffers 18  
19 and 20 of Manning cannot receive the output of OA1 because this output is not  
20 provided external to the standard voltage generator (VLG) of Fig. 27 of Kajigaya et  
21 al.

22 Hence, no combination of Manning and Kajigaya et al. by one of ordinary  
23 skill in the art at the time of the invention would have resulted in routing a random  
24 internal voltage level (i.e., the output of OA1 from between Q7 and Q55) out of the  
25 standard voltage generator (VLG) of Kajigaya et al. and providing this random

1 internal voltage level to the differential input buffers 18 and 20 of Manning. Thus, it  
2 is respectfully submitted that no combination of Manning and Kajigaya et al. can  
3 render the claimed invention obvious as represented by claim 1.

4 Accordingly, no art of record, either alone or in any combination, anticipates  
5 or renders obvious at least the following elements in conjunction with the other  
6 elements of their respective claims:

7 **Claim 1: one or more components, including a feedback component, that**  
8 **receive a distributed voltage . . . a voltage driver that produces a**  
9 **compensated voltage . . . wherein the compensated voltage is**  
10 **distributed to form the distributed voltage at the one or more**  
11 **components.**

12 **Claim 17: one or more data receivers that evaluate one or more**  
13 **corresponding data signals relative to a distributed reference**  
14 **voltage . . . a feedback receiver that evaluates the distributed**  
15 **reference voltage relative to a nominal reference voltage to**  
16 **produce a feedback signal . . . a reference voltage driver that**  
17 **produces a compensated reference voltage . . . wherein the**  
18 **compensated reference voltage is distributed to form the**  
19 **distributed reference voltage.**

20 **Claim 43: receiver means for evaluating a plurality of data signals**  
21 **relative to a distributed reference voltage . . . feedback means for**  
22 **evaluating the distributed reference voltage relative to a nominal**  
23 **reference voltage to produce a feedback signal . . . driver means**  
24 **having a variable gain for producing a compensated reference**  
25 **voltage . . . routing means for routing the compensated reference**



1 voltage on the integrated circuit to form the distributed reference  
2 voltage at the receiver and feedback means.

3 Claim 53: a plurality of data receivers that evaluate binary data signals  
4 with reference to a distributed reference voltage and that are  
5 coupled to the plurality of memory storage cells . . . a feedback  
6 receiver that evaluates the distributed reference voltage relative to  
7 a nominal reference voltage to produce a feedback signal . . . a  
8 reference voltage driver that produces a compensated reference  
9 voltage . . . wherein the compensated reference voltage is routed  
10 on the memory device to form the distributed reference voltage at  
11 the data and feedback receivers.

12 Claim 60: amplifying a nominal voltage by a variable gain to produce a  
13 compensated reference voltage . . . routing the compensated  
14 reference voltage over approximately impedance-matched  
15 resistive conductors to form a distributed voltage . . . evaluating a  
16 plurality of signals relative to the distributed voltage . . .  
17 evaluating the nominal voltage relative to the distributed voltage.

18 Claim 63: a reference voltage driver that has a variable gain and  
19 produces a compensated reference voltage . . . a plurality of  
20 receivers having substantially similar input characteristics that  
21 evaluate signals relative to a distributed reference voltage, a  
22 particular receiver of the plurality of receivers capable of  
23 evaluating a nominal reference voltage signal relative to the  
24 distributed reference voltage to produce a feedback signal . . .  
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wherein the compensated reference voltage is distributed to form  
the distributed reference voltage.

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1        **II. The rejection of at least claims 1, 17, 53, 60, and 63 under 35**  
2        **U.S.C. 103(a) appears to fail to directly address certain claim elements.**

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4        By way of example with respect to claim 1, the Office Action appears to fail  
5        to directly address **a nominal voltage**. Consequently, any element(s) of claim 1 that  
6        interact and/or interrelate with **a nominal voltage** are likewise not addressed.

7        It is therefore respectfully submitted that no complete rejection (e.g., no prima  
8        facie case under 35 U.S.C. §103(a)) has been instituted against at least claims 1, 17,  
9        53, 60, and 63. Thus, at least claims 1, 17, 53, 60, and 63 are allowable for this  
10       additional reason.

**CONCLUSION**

It is respectfully submitted that all of claims 1-73 are allowable, and prompt action to that end is hereby requested.

Respectfully Submitted,

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